REMARKS

The present application was filed on March 30, 2000 with claims 1 through 16. Claims 1 through 16 are presently pending in the above-identified patent application. Claims 1-9, 12, 15, and 16 are proposed to be amended herein.

In the Office Action, the Examiner rejected claims 1-16 under 35 U.S.C. §102(b) as being anticipated by Chung et al. (United States Patent Number 5,404,469).

The present invention is directed to a method and apparatus for allocating functional units in a multithreaded very large instruction word (VLIW) processor. The present invention combines the techniques of conventional VLIW architectures and conventional multithreaded architectures to reduce execution time within an individual program, as well as across a workload. The present invention utilizes a compiler to detect parallelism. The disclosed multithreaded VLIW architecture exploits program parallelism by issuing multiple instructions, in a similar manner to single threaded VLIW processors, from a single program sequencer, and also supports multiple program sequencers, as in simultaneous multithreading.

Independent Claims 1, 5, 9, 12, 15 and 16

Independent claims 1, 5, 9, 12, 15, and 16 were rejected under 35 U.S.C. §102(b) as being anticipated by Chung et al.

The Examiner asserts that Chung teaches an allocator for selecting and forwarding the instructions to the functional units based on the priority (col. 3, line 54, to col. 4, line 63; col. 3, lines 8-29; col. 7, lines 20-40; col. 8, lines 32-55).

Applicants note that, although Chung teaches that instructions are allocated to functional units, the allocation of instructions is not done independently. Chung teaches that "the processor 100 comprises four function units FU1, FU2, FU3, FU4. Illustratively, FU1 is an arithmetic unit, FU2 is a logic unit, FU3 is a load/store unit and FU4 is a branch unit." Col. 7, lines 43-46. Thus, each functional unit is *dedicated* to executing particular types of instructions and can therefore not be allocated independently. Independent claims 1, 5, 9, 12, 15, and 16, as amended, require independently allocating said functional units to any thread in said multithreaded instruction stream.

Thus, Chung et al. do not disclose or suggest independently allocating said functional units to any thread in said multithreaded instruction stream, as required by independent claims 1, 5, 9, 12, 15, and 16, as amended.

Dependent Claims 2-4, 6-8, 10-11 and 13-14

Dependent claims 2-4, 6-8, 10-11, and 13-14 were rejected under 35 U.S.C. §103(a) as being unpatentable over Chung et al.

Claims 2-4, 6-8, 10-11, and 13-14 are dependent on claims 1, 5, 9, and 12, respectively, and are therefore patentably distinguished over Chung et al. because of their dependency from amended independent claims 1, 5, 9, and 12 for the reasons set forth above, as well as other elements these claims add in combination to their base claim.

All of the pending claims, i.e., claims 1-16, are in condition for allowance and such favorable action is earnestly solicited.

If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this application, the Examiner is invited to contact the undersigned at the telephone number indicated below.

The Examiner's attention to this matter is appreciated.

Respectfully submitted,

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